REMARKS

The Applicant respectfully requests further examination and reconsideration in view of the amendments made above and the comments set forth below. Within the Office Action, claims 1-10 and 18-22 have been rejected. By the above amendment, claims 1, 5, 9, and 18 have been amended, and claims 23-28 have been added. Accordingly, claims 1-10 and 18-28 are pending.

Rejections under 35 U.S.C. § 112, first paragraph

Within the Office Action, claims 1-10 and 18-22 have been rejected under 35 U.S.C. 112, first paragraph. The Applicant respectfully disagrees.

Claims 1-10

As to claims 1-10, it is stated within the Office Action, "[T]he limitation 'wherein the first isolation technique and the second isolation technique are different and **implemented sequentially**' renders new matter situation" (bold and underlining in original). Furthermore, within the Office Action, in the section titled "Response to Arguments," it is stated that "the phrase 'the STI process is implemented on the silicon substrate prior to the LOCOS isolation' does not conclude the sequence of steps since some other intermediate steps may be formed therebetween."

The Applicant disagrees with this conclusion but, in order to further prosecution, has amended the independent claims 1 and 5 to both recite, "wherein the first isolation technique and the second isolation technique are different and implemented non-concurrently" (underlining added). Similarly, claim 9 has been amended to recite, "wherein the STI isolation technique and the LOCOS isolation technique are implemented non-concurrently (underlining added).

The claimed limitation "implemented non-concurrently" is not new matter; support for it can be found throughout the Specification as originally filed. For example, at page 4, lines 2-7 of the Specification, it is stated: "Preferably, the LOCOS isolation technique is first implemented to define a flash area of the silicon substrate on which the flash EPROM cell is implemented. . . . After the LOCOS isolation technique has been fully implemented, the flash area is then preferably masked and the STI technique is implemented in order to define the SRAM area of the silicon substrate on which the SRAM cell is implemented"; at page 8, lines 21-22: "In the preferred embodiment, the LOCOS isolation process is implemented on the substrate 100 before the STI process"; at page 9, lines 7-9: "Preferably after the LOCOS isolation process is completed, the STI process commences by forming a mask 170 over the second area 104 and an

active region within the first area 102, as illustrated in Figure 10"; on page 10, lines 5-7: "In the preferred embodiment of the present invention, the LOCOS isolation process is implemented on the silicon substrate before the STI process"; and on page 10, lines 9-10: "In a first alternate embodiment, the STI process is implemented on the silicon substrate prior to the LOCOS isolation process."

Because the limitations recited in claims 1, 5, and 9 find support in the Specification as filed, the rejection of these claims under 35 U.S.C. § 112, first paragraph, should be withdrawn.

Because claims 2-4 depend from claim 1, the rejection of these claims under § 112 should be withdrawn; because claims 6-7 depend from claim 5, the rejection of these claims under § 112 should be withdrawn; and because claim 10 depends from claim 9, the rejection of claim 10 under § 112 should also be withdrawn.

Claims 18-22

As to claims 18-22, it is stated within the Office Action, "[T]he limitation 'the first active region and the first isolation region forming a uniform region made of a first material, the second active region and the second isolation region forming a uniform region made of a second material,' renders new matter." The Applicant respectfully disagrees.

Nevertheless, to further prosecution of this case, claim 18 has been amended to recite, "the first isolation structure formed of a first material" and " the second isolation structure formed of a second material." Each of these limitations is supported in the specification as filed. For example, at page 9, lines 17-19, it is stated, with respect to the first limitation: "The shallow trenches 220 are then preferably filled with the insulating oxide substance 225 and a blanket etch is performed, as shown in Figure 14, to [remove a layer of oxide 110 and thus] expose the active regions 210 and 230." The isolation structure 220 is thus formed of a first material, the insulating oxide substance 225.

Similarly, with respect to the second limitation, it is stated at page 9, lines 3-4: "Next, as shown in Figure 9, the LOCOS isolation process is performed over the unmasked portions, forming field oxide layers 200." Later, as described at page 9, lines 12-13, a layer of nitride 120 on the field oxide layer 200 is etched away. As illustrated in Figure 14, the isolation structure 200 is thus formed of a second material, the field oxide 200.

Because the limitations "a first isolation structure formed of a first material" and "a second isolation structure formed of a second material" both find support in the specification, the Applicant respectfully requests that the rejection under 35 U.S.C. § 112, first paragraph, be withdrawn.

Furthermore, because claims 19-22 depend from claim 18, the rejection of these claims under § 112 should also be withdrawn.

Rejections under 35 U.S.C. § 103

Claims 1-10 and 18-22 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,605,853 to Yoo *et al.* (hereinafter "Yoo") in view of U.S. Patent No. 5,679,599 to Mehta (hereinafter "Mehta"). The Applicant respectfully disagrees with this rejection.

Yoo teaches a method of forming an SRAM, a floating gate memory, and a logic device on the same integrated circuit. Specifically, Yoo teaches a method of forming simultaneously a SRAM and an EEPROM on the same integrated circuit, using a LOCOS isolation process. (Yoo, col 3, lines 51-55). Yoo teaches a method of forming a plurality of field isolation regions using a LOCOS isolation process. (Yoo, col 3, line 55-60). Yoo does not teach or suggest that a SRAM and an EPROM can be formed on the same IC, using a non-LOCOS isolation process, such as a shallow trench isolation (STI) process. Neither does Yoo teach or suggest that a SRAM and an EPROM can be formed on the same IC, using a combination of a LOCOS and an STI isolation process.

Mehta teaches a device and method for isolating regions of the circuit device in a semiconductor substrate. The method comprises the following steps: forming a first insulation region and a second insulation region; etching a trench in the first insulation region, the trench extending into the semiconductor substrate to a depth below the surface of the substrate; filling the first isolation region with an isolation material and removing a portion of the isolation material such that the trench isolation material fills the trench and has a surface level with the surface of the substrate; and thermally growing a field oxide in the first and second isolation regions. (Mehta, Abstract and col. 4, line 46- col. 6, line 49). Mehta teaches a method of combining a LOCOS isolation process and structure, with a trench isolation process and structure, wherein a field oxide is grown which ***simultaneously*** forms a portion of the LOCOS region and trench isolation structure. (Mehta, col 4, line 47-51). However, Mehta does not teach or suggest combining a LOCOS isolation process and structure, with a trench isolation process and structure, wherein a field oxide is grown which *independently* or *non-concurrently* forms a portion of the LOCOS region and trench isolation structure. Furthermore, Mehta does not teach a separation technique for growing flash EPROM and SRAM on a common substrate.

Claims 1-10

The present invention is directed to a system for and method of integrating SRAM cells and flash EPROM cells onto a single silicon substrate including an area on the silicon substrate where a local oxidation of silicon (LOCOS) isolation technique is implemented and another area on the same silicon substrate where a shallow trench isolation (STI) technique is implemented. (Specification, Abstract). The present invention teaches a system for *independently* or *non-concurrently* integrating SRAM cells and flash EPROM cells onto a single silicon substrate.

As discussed above, Yoo does not teach or suggest that an SRAM and an EPROM can be formed on the same IC, using a non-LOCOS isolation process, such as a shallow trench isolation (STI) process. Nor does Yoo teach or suggest that a SRAM and an EEPROM can be formed on the same IC, using a combination of a LOCOS and STI isolation process. Within the Office Action, it is acknowledged that Yoo et al. do not expressly disclose a second isolation technique such as STI to isolate the devices.

Also, as discussed above, Mehta does not teach or suggest combining a LOCOS isolation process and structure, with a trench isolation process and structure, wherein a field oxide is grown which *independently* or *non-concurrently* forms a portion of the LOCOS region and trench isolation region. Nor does Mehta teach a separation technique for growing flash EPROM and SRAM on a common substrate. Accordingly, neither Yoo, Mehta nor their combination teach or suggest a system for independently or non-concurrently integrating SRAM cells and flash EPROM cells onto a single silicon substrate. Further, neither Yoo, Mehta nor their combination teach or suggest forming a SRAM and an EEPROM on a single substrate using a combination of a LOCOS and an STI isolation process.

Within the Office Action, it is recognized that "Yoo et al., however, does not expressly disclose a second isolation technique such as STI to isolate the devices." It is then stated that "Mehta, in fig. 18, teaches a first and second isolation techniques 242, 240 to separate the devices in the same substrate in order to scale the minimum spacing between regions" (citing Mehta, col. 6, last paragraph). It is then concluded that "it would have been obvious to one of ordinary skill in the art at the time of [sic] the invention was made to use STI isolation technique as taught by Mehta in Yoo et al. substrate in order to scale the minimum spacing between regions." The Applicant respectfully disagrees with this conclusion.

To support this conclusion, a *prima facie* case of obviousness must be demonstrated. No demonstration has been made here. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation demonstrated, either in the references themselves or in the knowledge generally available to one of ordinary skill in the

art, to combine the teachings of the references. Second, there must be a demonstration that the combination of the prior art references would result in a reasonable expectation of success. Third, the combination of the prior art references must teach or suggest all the claim limitations. [M.P.E.P § 2142 - 43.]

First, there is no suggestion or motivation to combine Yoo and Mehta. As discussed more fully below, Yoo teaches away from including a SRAM and an EPROM on the same IC, isolated by a combination of a LOCOS and a second isolation technique. Furthermore, Mehta does not teach or otherwise indicate that the first and second isolation techniques can be applied to isolate a SRAM and an EEPROM on a common IC. Therefore, it would not have been obvious to one skilled in the art to combine the teachings of Yoo and Mehta. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990). **Within the Office Action, there has not been any reference to any teaching, hint or suggestion in either Yoo or Mehta suggesting the desirability of combining these two references.**

Further, there is no indication in the prior art that a combination of Yoo and Mehta would result in a reasonable expectation of success. As indicated by Yoo, in column 2, lines 18-26, a combination of a SRAM and EEPROM on the same IC is desirable. *However, Yoo specifically teaches that such an IC is difficult to fabricate because of the difference in fabrication processes.* [Yoo, column 2, lines 23-26] Furthermore, the teachings of Mehta do not indicate or suggest that the first and second isolation techniques can be applied to isolate a SRAM and an EPROM on a common IC. The combination of the teachings of Yoo and Mehta would not have resulted in a reasonable expectation of success. Therefore, the combination of the teachings of Yoo and Mehta does not render the current invention obvious.

In contrast to the teachings of Mehta, Yoo and their combination, the present invention teaches a system for *independently* or *non-concurrently* integrating SRAM cells and flash EPROM cells onto a single silicon substrate. As discussed above, neither Mehta, Yoo nor their combination teaches or suggests forming a SRAM and an EPROM on a single substrate using a combination of a LOCOS and STI isolation process. In column 2, lines 18-26, Yoo states the following:

> It may be also desirable to form more than one type of memory structure on the same IC, such as an SRAM in conjunction with an EEPROM (Electrically Erasable Programmable Read Only Memory), as well as logic devices. However, such an IC is difficult to fabricate due to the difference in the typical processes for forming memory and logic and for forming significantly different memory devices.

This statement suggests that Yoo's invention is directed to a method of combining a SRAM and an EEPROM on the same IC, when the same LOCOS isolation process is used on all the regions of the substrate. By this statement, Yoo further concedes that his method does not solve the difficulty of fabricating an SRAM and an EPROM on the same substrate. Rather, Yoo suggests that an alternative to finding a method of combining two methods would be to improve the current LOCOS isolation method so as to be used on both the SRAM and EEPROM. Therefore, it would not have been obvious to one skilled in the art, that Yoo could have been combined with Mehta to disclose the current invention. Further, Yoo appears to be teaching away from using multiple different isolation processes on a single IC. Yoo acknowledges the inherent difficulty of applying multiple different isolation processes on an IC, and does not suggest or teach applying a LOCOS and STI isolation process on the same substrate. Therefore it would not have been obvious to one skilled in the art from the teachings of Yoo, that a LOCOS and STI isolation process could have been used to form a SRAM and an EEPROM on a common substrate.

Within the Office Action, the admonition is repeated that "Applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references." The Applicant has not attacked the references individually. The Applicant has continuously shown that neither the references nor their combination teach or make obvious the presently claimed invention. The Applicant has also continually shown that there is no motivation to combine the references into the combination used to reject the claims.

The independent Claim 1 is directed to a semiconductor device. The semiconductor device of Claim 1 comprises a common substrate, an SRAM device implemented on the common substrate and isolated by a first isolation technique and a flash EPROM device implemented on the common substrate and isolated by a second isolation technique. It is specified in claim 1 that the first isolation technique and the second isolation technique are different and implemented non-concurrently. As described above, neither Mehta, Yoo nor their combination, teach or suggest an SRAM device implemented on the common substrate and isolated by a first isolation technique and a flash EPROM implemented on the common substrate and isolated by a second isolation technique. Further, neither Mehta, Yoo nor their combination teach that the first

isolation technique and the second isolation technique are different and implemented non-concurrently. For at least these reasons, the independent claim 1 is allowable over the teachings of Mehta, Yoo and their combination.

Claims 2, 3 and 4 are dependent on the independent claim 1. As discussed above, the independent claim 1 is allowable over the teachings of Yoo, Mehta, and their combination. Claims 2, 3 and 4 are therefore allowable as being dependent on an allowable base claim.

The independent claim 5 is directed to a system for allowing different types of isolation techniques during fabrication of a semiconductor device. The system of claim 5 comprises a common substrate having a first portion on which a first isolation technique is implemented during processing and a second portion on which a second isolation technique is implemented during processing. It is specified in claim 5 that the first isolation technique and the second isolation technique are different and implemented non-concurrently. The system of claim 5 also includes an SRAM device implemented on the first portion of the substrate and a flash EPROM device, implemented on the second portion of the substrate. As discussed above, neither Mehta, Yoo nor their combination teach implementing an SRAM device, isolated by a first isolation technique, on a common substrate with a flash EPROM device, isolated by a second isolation technique. As further discussed above, neither Mehta, Yoo nor their combination teach that the first isolation technique and the second isolation technique are different and implemented non-concurrently. For at least these reasons, the independent claim 5 is allowable over the teachings of Mehta, Yoo and their combination.

Claims 6, 7, and 8 are all dependent on the independent claim 5. As discussed above, the independent claim 5 is allowable over the teachings of Mehta, Yoo and their combination. Accordingly, the dependent claims 6, 7 and 8 are also allowable as being dependent on an allowable base claim.

The independent claim 9 is directed to a semiconductor device comprising a common substrate having a first portion on which an STI isolation technique is implemented during processing and a second portion on which a LOCOS isolation technique is implemented during processing. It is specified in claim 9 that the STI isolation technique and the LOCOS isolation technique are implemented non-concurrently. The device of claim 9 also includes an SRAM device implemented on the first portion of the substrate and a flash EPROM device implemented on the second portion of the substrate. As described above, neither Mehta, Yoo, nor their combination teach implementing an SRAM device, isolated by an STI technique, on a common substrate with a flash EPROM device, isolated by a LOCOS isolation technique. As further discussed above, neither Mehta, Yoo nor their combination teach that the STI isolation technique

and the LOCOS isolation technique are implemented non-concurrently. For at least these reasons, the independent claim 9 is allowable over the teachings of Mehta, Yoo and their combination.

Claim 10 is dependent on the independent claim 9. As discussed above, the independent claim 9 is allowable over the teachings of Mehta, Yoo and their combination. Accordingly, the dependent claim 10 is also allowable as being dependent on an allowable base claim.

Within the Office Action, *In re Thorpe*, 777 F.2d 695, 227 U.S.P.Q. 964 (Fed. Cir. 1985), is cited for the assertion that a process limitation, such as the limitation "implemented non-concurrently" recited in amended claims 1, 5, and 9 "would not carry any patentable weight in this claim drawn to structure." Reliance on *Thorpe* is misplaced. In *Thorpe*, claim 1 was a process claim. 777. F.2d at 696. Claim 44, which was rejected, recited no structural limitations, claiming "The product of the process of Claim 1." *Id.* In contrast, claims of the present invention recite structure that is *further defined* by process limitations. For example, claim 1 of the present invention claims a common substrate; an SRAM device implemented on the common substrate and isolated by a first isolation technique; and a flash EPROM device implemented on the common substrate and isolated by a second isolation technique. Furthermore, the first isolation technique and the second isolation technique are different and implemented non-concurrently.

Claim 1, unlike the claim rejected in *Thorpe*, recites structure further defined by process steps. Accordingly, *Thorpe* does not teach against the limitations recited in claim 1.

Similarly, claims 5 and 9 also recite structure further defined by process limitations. For these reasons, claims 1, 5, and 9 are allowable in light of *Thorpe*.

As illustrated above, the Applicant has described both Yoo and Mehta, discussed the application of each, and argued why neither, alone or in combination, taught or suggested the invention claimed in the present application. Nevertheless, within the Office Action, the scope of the Applicant's arguments is ignored. As stated within the Office Action:

> Applicant repeatedly submits, "Yoo does not teach or suggest that a SRAM and an EEPROM can be formed on the same IC, using non-LOCOS isolation process, such as a shallow isolation (STI) process. Nor does Yoo teach or suggest that a SRAM and an EEPROM can be formed on the same IC, using a combination of a LOCOS and STI isolation process." As addressed in the previous Official Action, the combination of Yoo and Mehta teaches the technique of using LOCOS and STI isolations. The LOCOS and STI apparently are different. Applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the

> rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

This is a mischaracterization of the Applicant's arguments. Within the Office Action it is suggested that the Applicant argued only that Yoo does not disclose the claimed invention. As discussed above, however, the Applicant has argued and herein argues that neither Yoo nor Mehta, alone *or in combination*, teaches or suggests the claimed invention.

For this reason, the reliance on *Keller* and *Merck* within the Office Action is misplaced. In both *Keller* and *Merck*, the applicant tried to overcome a § 103 rejection by arguing that one reference did not teach a limitation taught in the pending application. In contrast, here the Applicant has described why the *combination* of references neither teaches nor suggests the claims in the present invention. Accordingly, the rejection of the independent claims 1, 5, and 9 is improper, and claims 1, 5, and 9 are allowable.

It is next stated within the Office Action:

> [The] applicant argues about the limitations of a method of making the device, on pages 5-6. It is noted that applicant elected the device claims in the previous amendment, paper 15. The method claims, Group II, therefore has [sic] been withdrawn from the examination. The newly added limitation such as implemented sequentially also is a process limitation[.] Thus, the device may be made of a different process, for example, simultaneously, as taught by Mehta, see sol, 4, lines 48-51.

The Applicant respectfully submits that the discussion of process limitations is relevant and, furthermore, that such claim limitations are allowable. First, the Applicant described the method of making the device to prove that neither Yoo nor Mehta, either alone or in combination, teaches how to make the present invention and thus cannot teach or suggest any combination that would produce the present invention. As stated in the Response to Office Action Mailed on May 6, 2002:

> The discussion within the previous Responses on the limitations of the LOCOS and STI isolation techniques is relevant since it limits the applicability of the teachings of Yoo in view of Mehta, to the present invention. It is relevant because, without incorporating two separate techniques independently or sequentially, neither Yoo, Mehta, nor their combination can teach the claimed invention, which expressly teaches the incorporation of two separate techniques in the fabrication of the claimed invention.

Second, the MPEP itself allows product-by-process claims: "A product-by-process claim, which is a product claim that defines the claimed product in terms of the process by which it is made, is proper." MPEP § 2173.05(p)(I) (8th ed. 2001).

The Applicant submits that the claim limitation "implemented non-concurrently" properly helps define the Applicant's invention and, further, distinguishes the Applicant's invention over the prior art. For at least this reason, claims 1-10 are allowable.

Claims 18-22

Within the Office Action, claims 18-22 have been rejected under 35 U.S.C. § 103 as being unpatentable over Yoo in view of Mehta. The Applicant respectfully disagrees.

Claim 18 is directed to a semiconductor device comprising a common substrate, a first region formed on the common substrate, and a second region formed on the common substrate. The first region comprises an SRAM device, a first active region, and a first isolation region having a first isolation structure. The first isolation structure is formed of a first material. The SRAM device overlies the first active region, which is isolated by the first isolation structure. The second region comprises a flash EPROM device, a second active region, and a second isolation region having a second isolation structure. The second isolation structure is formed of a second material. The flash EPROM device overlies the second active region, which is isolated by the second isolation structure. It is specified in claim 18 that the first isolation structure is contiguous to and different from the second isolation structure.

Neither Mehta, Yoo, nor their combination teaches or suggests two different and contiguous isolation structures, each made of a single material. For at least this reason, claim 18 distinguishes over Mehta, Yoo, and their combination, and is allowable. Similarly, because claims 19-22 depend from claim 18, they too are allowable as depending from an allowable base claim.

The added limitation that the first isolation structure and the second isolation structure are contiguous finds support in the specification at, for example, Figure 14 and the accompanying text.

The new claims 23-28 are allowable over the prior art.

The new claim 23 is directed to a semiconductor device comprising a common substrate, an SRAM device, and a flash EPROM device. The SRAM device is implemented on the common substrate and formed over a first active region on a first isolated structure. The flash EPROM device is implemented on the common substrate and formed over a second active region

on a second isolated structure. The second isolated structure has a first portion extending a first depth into the substrate and a second portion containing the second active region and extending a second depth into the substrate. The first depth larger than the second depth. Furthermore, the first isolated structure and the second isolated structure are different. A device having a first depth and a second depth as recited in claim 23 allows for efficient device isolation, and thus allows for a more densely populated semiconductor device.

Mehta, in Figure 18 and the accompanying text, discloses a circuit device having a field oxidized trench region 242 and a conventional LOCOS region 240 having a bird's beak. The trench region 242 and the LOCOS region 240 are further isolated by a portion of both the oxide layer 110 and the nitride layer 120. As recognized in the pending application, for example at page 2, lines 16-21, and at page 3, lines 2-4, a bird's beak structure does not effectively isolate active portions of a semiconductor device and thus does not allow for smaller device spacing. Mehta teaches that nitride spacers 180a can be used to reduce, but not eliminate, the bird's beak effect. (Mehta, col. 6, lines 36-42) Mehta does not teach an isolation structure as claimed in claim 23, having a first portion extending a first depth and a second portion extending a second depth smaller than the first depth. For at least this reason, claim 23 is distinguishable over Mehta.

Similarly, Yoo does not teach an isolation structure as taught in claim 23, having a first portion extending a first depth and a second portion extending a second depth smaller than the first depth. For at least this reason, claim 23 is distinguishable over Yoo.

Because claim 23 recites structure neither taught nor suggested by Mehta, Yoo, or their combination, claim 23 is allowable over Mehta and Yoo. Furthermore, because claims 24 and 25 depend from claim 23, they too are allowable over Mehta and Yoo.

Claim 26 is directed to a system containing a semiconductor device having a plurality of isolated structures. The system comprises a common substrate having a first portion on which a first isolation technique is implemented during processing and a second portion on which a second isolation technique is implemented during processing. The first portion contains a first active region. The second portion has a first segment extending a first depth into the substrate and a second segment containing a second active region extending a second depth into the substrate. The first depth is larger than the second depth. The first isolation technique and the second isolation technique are different. An SRAM device is implemented on the first active region on the first portion of the substrate, and a flash EPROM device implemented on the second active region on the second portion of the substrate.

The system of claim 26 includes an isolation structure having two depths, a structure that efficiently allows for device separation and thus allows for a more densely populated semiconductor device. Thus, claim 26 is allowable over Mehta, Yoo, and their combination, for at least the same reasons that claim 23 is allowable. Similarly, because claims 27 and 28 depend from claim 23, they too are allowable as depending from an allowable base claim.

The limitations recited in both claims 23 and 26 find support throughout the specification as filed, for example, in Figure 14 and the accompanying text.

For the reasons given above, the Applicant respectfully submits that claims 1-10 and 18-28 are in a condition for allowance, and allowance at an early date would be appreciated. If the Examiner has any questions or comments, the Examiner is encouraged to call the undersigned at (408) 530-9700 to discuss them so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
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Dated: June 26, 2003

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